United States Patent and Trademark Office

Application No.:	10/709,844
Confirmation No.:	3843
Filed:	June 1, 2004
First Named Inventor:	Graham Balsdon
Title:	Automatic Routing System with Variable Width Interconnect
Examiner:	Naum B. Levin
Art Unit:	2825
Customer No.:	51111
Docket No.:	21648–000700

Commissioner for Patents
POB 1450
Alexandria, VA 22313-1450

Appellant's Brief in Support of Appeal Under 37 C.F.R. § 1.191

Dear Commissioner:

This is an appeal brief in support of an appeal from the final office action (rejecting claims 1–5, 7–14, and 21–30), mailed March 22, 2007, and Notification of Panel Decision from Pre–Appeal Brief Review, mailed August 24, 2007. The following items are included in this brief:

Real Party in Interest

The real party in interest is Pulsic Limited of the United Kingdom, which is the assignee of record.

Related Appeals and Interferences

Appellant is not aware of any related appeals or interferences.

Status of Claims

Claims 1–5, 7–14, and 21–30 are pending in this application. Claims 6 and 15–20 are canceled.

Claims 1–5, 7–14, and 21–30 are rejected and the subject of this appeal.

A claims appendix to this appeal brief contains a listing of the pending claims.

Status of Amendments

On March 22, 2007, the examiner mailed a final rejection. On June 22, 2007, appellant submitted an amendment to the claims. On July 5, 2007, in an advisory action, the examiner reported that the amendments to the claims were to be entered.

Summary of the Claimed Subject Matter

The present invention provides a system and technique for automatically routing interconnect lines, where each interconnect line can include segments which are different widths. Paragraphs 8, 72, 80, 82, 84, 93, 98, and 100. A system has a mouse, graphical user interface tool, and access to a database. Figures 1–3 and paragraphs 23–28. In an embodiment, the system includes a shape-based automatic router tool. Figure 3 and paragraphs 29–31. For shape-based routing, flooding operations are used to create an interconnect route path. Paragraph 30. The routing tool has access to the extraction information, so that based on this extracted information, track segments are created with a certain width (which may vary) as needed to address issues such as current density or optical proximity (OPC) rules. Paragraphs 42–45 and 73. A single net may include segments, each having a different width. Figure 4 and paragraphs 80, 82, 84, 93, 96–98, and 100. The router may widen or not widen based on design rules. Paragraph 75.

Information on nets may be provided by way of files or tables such as a current density table. Paragraphs 86–87. Frequencies for nets may be provided in a file and if not provided, DC operation is assumed, or a warning message is displayed. Paragraph 89. Routing may be performed using a Steiner tree approach (paragraphs 102 and 128) or a batched greedy algorithm (paragraph 129 and 148–152).

Grounds of Rejection to Be Reviewed on Appeal

I. A first ground of rejection to be reviewed on appeal involves whether claims 1, 5, 7–11, 13–14, and 21–22 are under 35 U.S.C. § 102(e) unpatentable over U.S. patent publication 20060080630 (Lin).

II. A second ground of rejection to be reviewed on appeal involves whether claims 2–4 and 24–27 are under 35 U.S.C. § 103(a) unpatentable over U.S. patent publication 20060080630 (Lin) in view of U.S. patent 5,737,580 (Hathaway).

III. A third ground of rejection to be reviewed on appeal involves whether claims 23 and 28–29 are under 35 U.S.C. § 103(a) unpatentable over U.S. patent publication 20060080630 (Lin) in view of Balakrishnan et al. ("A Greedy Router with Technology Targetable Output").

IV. A fourth ground of rejection to be reviewed on appeal involves whether claims 12 and 30 are under 35 U.S.C. § 103(a) unpatentable over U.S. patent publication 20060080630 (Lin) in view of U.S. patent 6,109,775 (Tripathi).

Argument

I. Argument Against First Ground of Rejection

Claims 1, 5, 7–11, 13–14, and 21–22 were rejected under 35 U.S.C. § 102(e) as being unpatentable over U.S. patent publication 20060080630 (Lin). Appellant believes this rejection is improper for the reasons discussed below.

For this argument, the claims are grouped as follows:

Group I.1: Claims 1, 7, 8, and 22 stand or fall together.

Group I.2: Claim 5 stands or falls by itself.

Group I.3: Claims 9–11 and 13–14 stand or fall together.

Group I.4: Claim 21 stands or falls by itself.

Group I.5: Claim 22 stands or falls by itself.

Group I.1: Claims 1, 7, 8, and 22

Claim 1 recites "a *shape-based automatic router tool*, capable of accessing the database, *using flood operations to create an interconnect route path* for at least one net of the integrated circuit design, selected using the graphical user interface tool and the mouse, wherein the interconnect route path comprises *segments having different interconnect widths*."

Lin does not show or suggest a shape-based automatic router tool which uses flood operations. Rather, as described at paragraph 47, Lin's tool employs "*a coordinate system, such as an X-Y Cartesian coordinate system*, to identify the placement, movement and orientation of the blocks relative to the floor plan design." Therefore, Lin describes a gridded design tool, which is unlike a shape-based or gridless tool of the invention. For at least this reason, claim 1 should be allowable.

Furthermore, at paragraph 110, Lin describes using "channel boxes" to perform power and ground line routing. In Lin, a channel box is the box formed by the channels of empty area between the blocks. Figure 7 shows examples of channel boxes, indicated by reference numbers 711F and 711G, into which wires are inserted.

A flood operation of the invention, however, is something different from Lin's channel box. Shape-based or gridless routing and flooding is described in the present application at, for example, paragraphs 29–31. See also figure 7 of the present patent application for an example. First, the flooding operation is gridless while Lin uses a gridded approach.

Second, flooding operations are used to expand an edge of a polygon until the flood reaches an obstacle. Once an obstacle is reached, the flood operation floods around the obstacle. The flood operation may make turns, such as 90 degree or other angles, to route around the obstacle. A track routed through flooding operations follows the flood, from the starting edge to the ending edge.

The channel boxes in Lin are unlike floods (resulting from flooding operations) of the invention. Nowhere does Lin discuss flooding to an obstacle or flooding around obstacles by making turns. The channel boxes are simply rectangular boxes of empty areas, which is different from flooding. Unlike floods, these boxes do not extend until they hit an obstacle. For example, in figure 7, see 711A, which does not extend until it hits block 709, but is separated from 709 by another box 711G. See 711D which does not extend until it hits box 711E, but is separated from 711E by another box 711G.

Also, the tracks within the boxes in Lin have bends and jogs (e.g., see 711F and 711G), but these do not result from flooding because the tracks do not follow a path created the channel boxes. Further, within the channel boxes 711F and 711G, there are three tracks connecting to X points which are clearly not the result of flooding. If the channel box were a flood, the track would go from one edge to another, and not go from one edge to two different edges (i.e., Xs on three different edges), as in Lin. Therefore, Lin's channel boxes are not floods like in the invention. (Compare to how tracks are created in figure 7 of the present patent application.)

For at least this additional reason, claim 1 should be allowable. Claims 2–8 and 21–22 are dependent on claim 1 and should be allowable for at least similar reasons as discussed in this group. Claims 9–12 and 13–14 recite "at least one flooding operation" and should be allowable for at least the similar reasons as discussed in this group.

Further, some of the claims in this group include limitations discussed in other groups. These claims should be allowable for at least the reasons discussed in this group and for the additional reasons discussed in other groups.

Group I.2: Claim 5

Claim 5 recites "wherein the shape-based automatic router tool uses at least one of *Steiner tree algorithm*, heuristic Steiner tree creation algorithm, or *batched greedy algorithm*." The examiner cited paragraph 133 of Lin as showing this feature of the invention. However, paragraph 133 and no other paragraphs in Lin discuss Steiner trees or a batched greedy algorithm. Lin cannot anticipate a claim which has claim elements it does not teach.

For at least this reason, claim 5 should be allowable. Claim 5 incorporates the limitations of claim 1 and should be allowable for at least similar reasons as discussed in group I.1 above. See also section III below for discussion on the batched greedy algorithm.

Group I.3: Claims 9–11 and 13–14

Claim 9 recites:

> using at least one *flooding operation* to determine an *interconnect route path* between a first point and a second point of an integrated circuit design;
>
> *comparing a property of the interconnect route path to a design rule*;

if the property of the first interconnect path violates the design rule, *creating an interconnect line for the interconnect route path having a first width*; and

if the property of the first interconnect path meets the design rule, *creating the interconnect line for the interconnect route path having a second width*, different from the first width.

The present invention, as claimed, is different from Lin. Starting a paragraph 121, Lin describes a power and ground wire optimization tool. This tool takes wires that already have been created, such as by a routing process, and optimizes these wires, such as widening a wire.

The invention provides a routing tool which uses *flooding* (not taught by Lin for the reasons discussed in I.1 above) to determine a route path. *Before creating the interconnect line, a property of the route path is compared against a design rule*. Based on this comparison, the interconnect line is *created with a first width or second width*, where these widths are different from each other. Therefore, the invention provides an automatic routing tool which creates wires having varying widths.

The approach of the invention is different from Lin. In Lin, the *routing tool* does nothing to adjust the widths of the wires. See paragraphs 108–120. Only the *wire optimization tool* (paragraphs 121–142) adjusts wire width, and this occurs only after the wires have been routed. The invention provides the benefit that as wires gets routed and created by the *routing tool*, width adjustments can be made. Subsequently routed paths can be adjusted as needed to take into account previously routed wires. Lin cannot do this because all the wires are already created when the wire optimization tool is used.

For at least this reason, claim 9 is allowable. Claims 10–12 are dependent on claim 9 and should be allowable for at least similar reasons as discussed in this group. Claims 13–14 also should be allowable for at least the similar reasons as discussed in this group.

Further, some of the claims in this group include limitations discussed in other groups (e.g., "flooding operation" is discussed in group I.1 above). These claims should be allowable for at least the reasons discussed in this group and for the additional reasons discussed in other groups.

Group I.4: Claim 21

Claim 21 recites:

> wherein automatic router tools creates *interconnect route paths for a first net, a second net, and a third net, each of the first, second, and third nets carrying different signals*, and the first net comprises segments having *different interconnect widths*, the signal net comprises segments having *different interconnect widths*, and the third net comprises segments having *different interconnect widths*.

The invention is a shape-based automatic router tool to route signal nets of an integrated circuit. In contrast, Lin is wire routing correction and optimization tool for power and ground wires. See title, summary, and paragraphs 76 (defining a "PG network") and 125–132. At best, Lin describes an approach for power and ground wires, which are *not signal nets* as recited in the claim.

And to be sure, Lin does not show or suggest creating interconnect route paths for *three nets* carrying *three different signals*, especially where the three nets have segments with *different widths*. Lin's approach is for (i) power and (ii) ground wires (which are not signal nets), no other wires. Certainly, Lin does not show or suggest an approach for *three nets carrying three different signals* as recited in the claim.

For at least this reason, claim 21 should be allowable. Also, claim 21 incorporates the limitations of claim 1 and should be allowable for at least similar reasons as discussed in group I.1 above.

Group I.5: Claim 22

Claim 22 recites "wherein the automatic router tool performs *detailed routing*." At paragraph 62–63, 64, and 73, Lin describes using global routing for Lin's power and ground routing approach, rather than detailed routing because detailed routing is typically very time consuming (see paragraph 8). So, Lin acknowledges the existence of detailed routing, but chooses to *teach away* from using it.

The invention is the opposite of Lin. In an embodiment, the automatic router tool of the invention performs detailed routing, something which is discouraged and not taught by Lin.

For at least this reason, claim 22 should be allowable. Also, claim 22 incorporates the limitations of claim 1 and should be allowable for at least similar reasons as discussed in group I.1 above.

II. Argument Against Second Ground of Rejection

Claims 2–4 and 24–27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent publication 20060080630 (Lin) in view of U.S. patent 5,737,580 (Hathaway). Appellant believes this rejection is improper for the reasons discussed below.

For this argument, the claims are grouped as follows:

Group II.1: Claims 2 and 24 stand or fall together.

Group II.2: Claims 3 and 26 stand or fall together.

Group II.3: Claims 4 and 27 stand or fall together.

Group II.4: Claim 25 stands or falls by itself.

Group II.1: Claims 2 and 24

Claim 2 recites:

> a file, accessible by the shape-based automatic router tool, comprising a *current density table* comprising *current density as a function of* at least one of layer, net frequency, or track width.

The examiner asserts that Hathaway shows or suggests this feature of the invention. But, at column 5, lines 34–52, Hathaway provides an equation used to define a maximum downstream capacitance, not a table including current densities. A capacitance equation is different from a current density table. A current density table relates current density (e.g., amperes per cross-sectional area) to, for example, net frequency, while Hathaway's equation provides a capacitance value (e.g., farads). Even if one were to tabulate values using Hathaway's capacitance table, and there is no suggestion that this should be done, the result still *would not be a current density table.*

Further, the examiner states that reducing capacitive effects reduces current density, but this is not what is recited in the claim language. The claim cites a table of current densities as related to net frequency. Other relationships not shown or suggested include a table of current

densities as related to layer (e.g., which layer of metal such as metal-1 or metal-2) and as related to track width.

For at least this reason, claims 2 and 24 should be allowable. Further, some of the claims in this group include limitations discussed in other groups (e.g., "shaped-based automatic router tool" is discussed in group I.1 above). These claims should be allowable for at least the reasons discussed in this group and for the additional reasons discussed in other groups.

Group II.2: Claims 3 and 26

Claim 3 recites:

> a file, accessible by the shape-based automatic router tool, *comprising frequency information for one or more nets* of integrated circuit, wherein *when frequency information is not provided for a net, DC operation of the net will be assumed.*

A typical integrated circuit will have a number of nets. In the invention as claimed, there is a file having frequency information for the nets, and when frequency information is not in the file, DC operation of a net is assumed. Hathaway does not show or suggest such a file and does not discuss making such an assumption. At column 5, lines 34–52 (discussed in group II.1 above), an equation for capacitance is provided, but nothing about a file with frequency values.

With the invention, the file allows faster routing of nets, while the prior art make calculations, determining frequencies using simulation or equation, which are much more time consuming. And for the invention, when a frequency is not in the file, DC operation is assumed. This can facilitate routing of a more quickly, while for the prior art, calculations or simulations are made (e.g., to determine a frequency of the net and to calculate any changes to the wiring) since DC operation is not assumed. Thus, the invention provides a way to improve routing speed.

For at least this additional reason, claims 3 and 26 should be allowable. Further, some of the claims in this group include limitations discussed in other groups (e.g., "shaped-based automatic router tool" is discussed in group I.1 above). These claims should be allowable for at least the reasons discussed in this group and for the additional reasons discussed in other groups.

Group II.3: Claims 4 and 27

Claim 4 recites:

> a file, accessible by the shape-based automatic router tool, *comprising frequency information for one or more nets of integrated circuit*, wherein *when frequency information is not provided for a net, a warning message is presented.*

As discussed for group II.2 above, Hathaway does not show or suggest a file as recites. Hathaway also does not show or suggest presenting a warning message when frequency information is not provided for a net. The invention is able to detect potential missing input information, which the prior art does not consider.

For at least this reason, claims 4 and 27 should be allowable. Further, some of the claims in this group include limitations discussed in other groups (e.g., "shaped-based automatic router tool" is discussed in group I.1 above). These claims should be allowable for at least the reasons discussed in this group and for the additional reasons discussed in other groups.

Group II.4: Claim 25

Claim 25 recites "*a file, accessible by the shape-based automatic router tool, comprising frequency information for one or more nets of integrated circuit.*"

As discussed in group II.2 above, Hathaway does not show or suggest a file as recited. With the invention, the file allows faster routing of nets, while the prior art make calculations, determining frequencies using simulation or equation, which are much more time consuming.

For at least this reason, claim 25 should be allowable. Further, claim 25 includes limitations discussed in other groups (e.g., "shaped-based automatic router tool" is discussed in group I.1 above). Claim 25 should be allowable for at least the reasons discussed in this group and for the additional reasons discussed in other groups.

III. Argument Against Third Ground of Rejection

Claims 23 and 28–29 are 35 U.S.C. § 103(a) were rejected over U.S. patent publication 20060080630 (Lin) in view of Balakrishnan et al. ("A Greedy Router with Technology Targetable Output"). Appellant believes this rejection is improper for the reasons discussed below.

Claim 24 recites "a file, accessible by the shape-based automatic router tool, comprising *a current density table comprising current density as a function of net frequency*." Claim 28 is dependent on claim 28 and recites ""*wherein the shape-based automatic router tool uses a batched greedy algorithm to create the interconnect route path*."

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1734, 82 U.S.P.Q.2d 1385, 1391 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18, 148 U.S.P.Q. 459, 467 (1966). Secondary considerations such as commercial success, long felt but unsolved needs, failure of others, and so forth, "might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented." 383 U.S. at 18, 148 U.S.P.Q. at 467. See also *KSR*, 127 S.Ct. at 1734, 82 U.S.P.Q.2d at 1391 ("While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.").

Lin and Balakrishnan describe completely different approaches to routing and it is *not obvious to combine* the references in a way to make the invention. Lin describes a grid-based automatic router approach (discussed in I.1 above), while Balakrishnan describes a gridless CDL environment and the difficulties of reconciling these environments. Balakrishnan, introduction.

As evidenced by Balakrishnan, the CDL environment does not consider any parameters regarding the specific performance attributes of the nets (such as frequency information) and altering net width based on such attributes during routing. Even Lin does not consider the performance attributes of the power and ground wires during the automatic routing phase (discussed above), but rather through using a separate optimization tool after the wire routing is completed. Combining Lin and Balakrishnan will not result in an automatic router tool that considers performance attributes (such as net frequency) during the routing phase. That result is simply something which is not rendered obvious by the prior art.

For at least this reason, claims 23 and 28–29 should be allowable. Further, some of the claims in this group include limitations discussed in other groups (e.g., "shaped-based automatic router tool" is discussed in group I.1 above). These claims should be allowable for at least the reasons discussed in this group and for the additional reasons discussed in other groups.

IV. Argument Against Fourth Ground of Rejection

Claims 12 and 30 were rejected under 35 U.S.C. § 103(a) unpatentable over U.S. patent publication 20060080630 (Lin) in view of U.S. patent 6,109,775 (Tripathi). Appellant believes this rejection is improper for the reasons discussed below.

Claim 30 recites:

> *automatically determining an interconnect route path* between a first point and a second point of an integrated circuit design;
>
> determining a *property of the interconnect route path*; and
>
> *creating an interconnect line for the interconnect route path having a width based on the property of the interconnect route path and optical proximity effects.*

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1734, 82 U.S.P.Q.2d 1385, 1391 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18, 148 U.S.P.Q. 459, 467 (1966). Secondary considerations such as commercial success, long felt but unsolved needs, failure of others, and so forth, "might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented." 383 U.S. at 18, 148 U.S.P.Q. at 467. See also *KSR*, 127 S.Ct. at 1734, 82 U.S.P.Q.2d at 1391 ("While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.").

Although both references are in the electronic design automatic area, for one of skill in this art, Lin and Tripathi discuss completely different subject matter. Lin describes an automatic router and a power and ground optimization tool, while Tripathi describes a method of to reduce processing patterning problems such as optical proximity effects.

Tripathi's approach is to alter wires of a layout, but this is performed well after the wires have already been routed. In fact, unless the wires are already placed, Tripathi would not know where dummy lines or other changes are needed. See Tripathi, column 13, line 64 to column 6, line 51. So, Tripathi makes compensating changes to the wires that are already routed and placed in the layout.

Combining Lin and Tripathi will not result in an automatic router tool that considers optical proximity effects *during the routing and creating of the wire.* Lin's approach may be used first, then followed by Tripathi's approach, but this is not the invention as recited. The invention provides a technique of considering and addressing issues such as optical proximity effects during the automatic routing operation.

For at least this reason, claims 12 and 30 should be allowable. Further, some of the claims in this group include limitations discussed in other groups (e.g., "shaped-based automatic router tool" is discussed in group I.1 above). These claims should be allowable for at least the reasons discussed in this group and for the additional reasons discussed in other groups.

Conclusion

For the above reasons, appellant submits that the examiner's rejections of the claims should be withdrawn, and reversal of the examiner's decision is respectfully requested.

Respectfully submitted,

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Attachments: Claims Appendix
Evidence Appendix
Related Proceedings Appendix

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Claims Appendix

1. An electronic automation system comprising:

a database of an integrated circuit design;

a mouse input device;

a graphical user interface tool, capable of accessing and performing operations on the database, based on input from the mouse input device; and

a shape-based automatic router tool, capable of accessing the database, using flood operations to create an interconnect route path for at least one net of the integrated circuit design, selected using the graphical user interface tool and the mouse, wherein the interconnect route path comprises segments having different interconnect widths.

2. The system of claim 1 further comprising:

a file, accessible by the shape-based automatic router tool, comprising a current density table comprising current density as a function of at least one of layer, net frequency, or track width.

3. The system of claim 1 further comprising:

a file, accessible by the shape-based automatic router tool, comprising frequency information for one or more nets of integrated circuit, wherein when frequency information is not provided for a net, DC operation of the net will be assumed.

4. The system of claim 1 further comprising:

a file, accessible by the shape-based automatic router tool, comprising frequency information for one or more nets of integrated circuit, wherein when frequency information is not provided for a net, a warning message is presented.

5. The system of claim 1 wherein the shape-based automatic router tool uses at least one of Steiner tree algorithm, heuristic Steiner tree creation algorithm, or batched greedy algorithm.

7. The system of claim 1 wherein the integrated circuit design comprises at least one of a memory integrated circuit, DRAM, EPROM, EEPROM, Flash memory, ASIC, microprocessor, programmable logic device, field programmable gate array, digital signal processor, analog integrated circuit, amplifier circuit, system on a chip, or programmable system-on-a-chip.

8. The system of claim 1 wherein shape-based automatic router tool creates interconnect route paths for two or more nets, and the interconnect route paths are for one layer of the integrated circuit design.

9. A method of designing an integrated circuit comprising:

using at least one flooding operation to determine an interconnect route path between a first point and a second point of an integrated circuit design;

comparing a property of the interconnect route path to a design rule;

if the property of the first interconnect path violates the design rule, creating an interconnect line for the interconnect route path having a first width; and

if the property of the first interconnect path meets the design rule, creating the interconnect line for the interconnect route path having a second width, different from the first width.

10. The method of claim 9 wherein the property is a current requirement of the interconnect route path.

11. The method of claim 9 wherein the design rule is a current density rule.

12. The method of claim 9 wherein the design rule is an optical proximity effect correction rule.

13. A method of designing an integrated circuit comprising:

using at least one flooding operation to determine an interconnect route path between a first point and a second point of an integrated circuit design;

determining a property of the interconnect route path; and

creating an interconnect line for the interconnect route path having a width based on the property of the interconnect route path and a design rule.

14. (original) The method of claim 13 wherein the design rule addresses at least one of current density, optical proximity effects, current handling, power handling, reliability, electromigration, voltage drop, or self-heating.

21. The system of claim 1 wherein automatic router tools creates interconnect route paths for a first net, a second net, and a third net, each of the first, second, and third nets carrying different signals, and

the first net comprises segments having different interconnect widths, the signal net comprises segments having different interconnect widths, and the third net comprises segments having different interconnect widths.

22. The system of claim 1 wherein the automatic router tool performs detailed routing.

23. An electronic design automation system comprising:

a database of an integrated circuit design;

a mouse input device;

a graphical user interface tool, capable of accessing and performing operations on the database, based on input from the mouse input device; and

an automatic shape-based router tool, capable of accessing the database, using a batched greedy algorithm to create an interconnect route path for at least one net of the integrated circuit design, selected using the graphical user interface tool and the mouse, wherein the interconnect route path comprises segments having different interconnect widths.

24. An electronic automation system comprising:

a database of an integrated circuit design;

a mouse input device;

a graphical user interface tool, capable of accessing and performing operations on the database, based on input from the mouse input device;

a shape-based automatic router tool, capable of accessing the shape-based database, to create an interconnect route path for at least one net of the integrated circuit design, selected using the graphical user interface tool and the mouse, wherein the interconnect route path comprises segments having different interconnect widths; and

a file, accessible by the shape-based automatic router tool, comprising a current density table comprising current density as a function of net frequency.

25. An electronic automation system comprising:

a database of an integrated circuit design;

a mouse input device;

a graphical user interface tool, capable of accessing and performing operations on the database, based on input from the mouse input device;

a shape-based automatic router tool, capable of accessing the shape-based database, to create an interconnect route path for at least one net of the integrated circuit design, selected using the graphical user interface tool and the mouse, wherein the interconnect route path comprises segments having different interconnect widths; and

a file, accessible by the shape-based automatic router tool, comprising frequency information for one or more nets of integrated circuit.

26. The system of claim 25 wherein when frequency information is not provided for a net, DC operation of the net will be assumed.

27. The system of claim 25 wherein when frequency information is not provided for a net, a warning message is presented.

28. The system of claim 24 wherein the shape-based automatic router tool uses a batched greedy algorithm to create the interconnect route path.

29. The system of claim 25 wherein the shape-based automatic router tool uses a batched greedy algorithm to create the interconnect route path.

30. A method of designing an integrated circuit comprising:

automatically determining an interconnect route path between a first point and a second point of an integrated circuit design;

determining a property of the interconnect route path; and

creating an interconnect line for the interconnect route path having a width based on the property of the interconnect route path and optical proximity effects.

Evidence Appendix

None

Related Proceedings Appendix

None